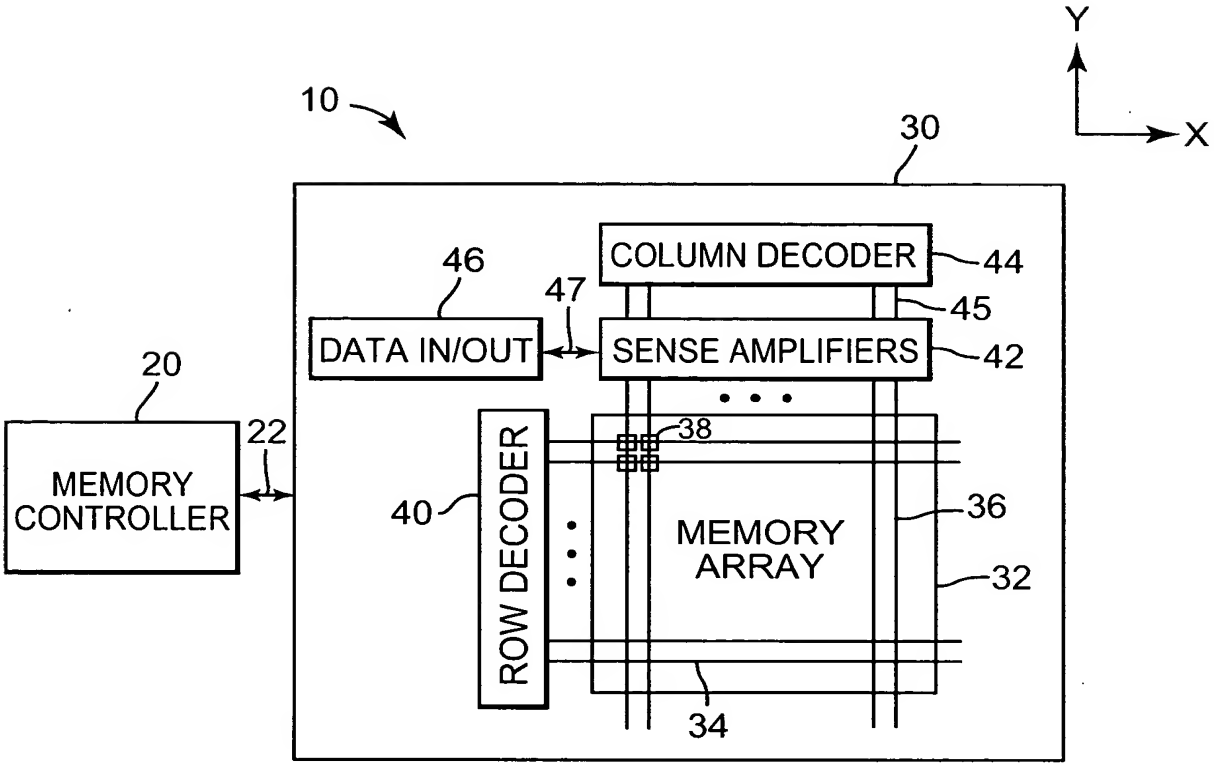
Y
X
10
30
COLUMN DECODER
44
46
47
45
DATA IN/OUT
SENSE AMPLIFIERS
42
20
22
38
MEMORY CONTROLLER
40
ROW DECODER
MEMORY ARRAY
36
32
34

Fig. 1

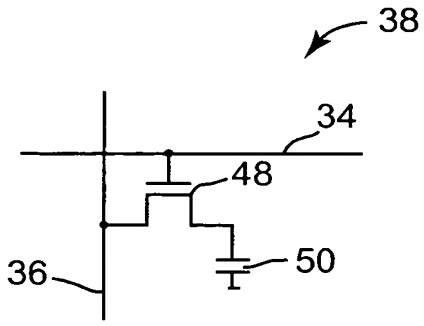
38
34
48
50
36

Fig. 2

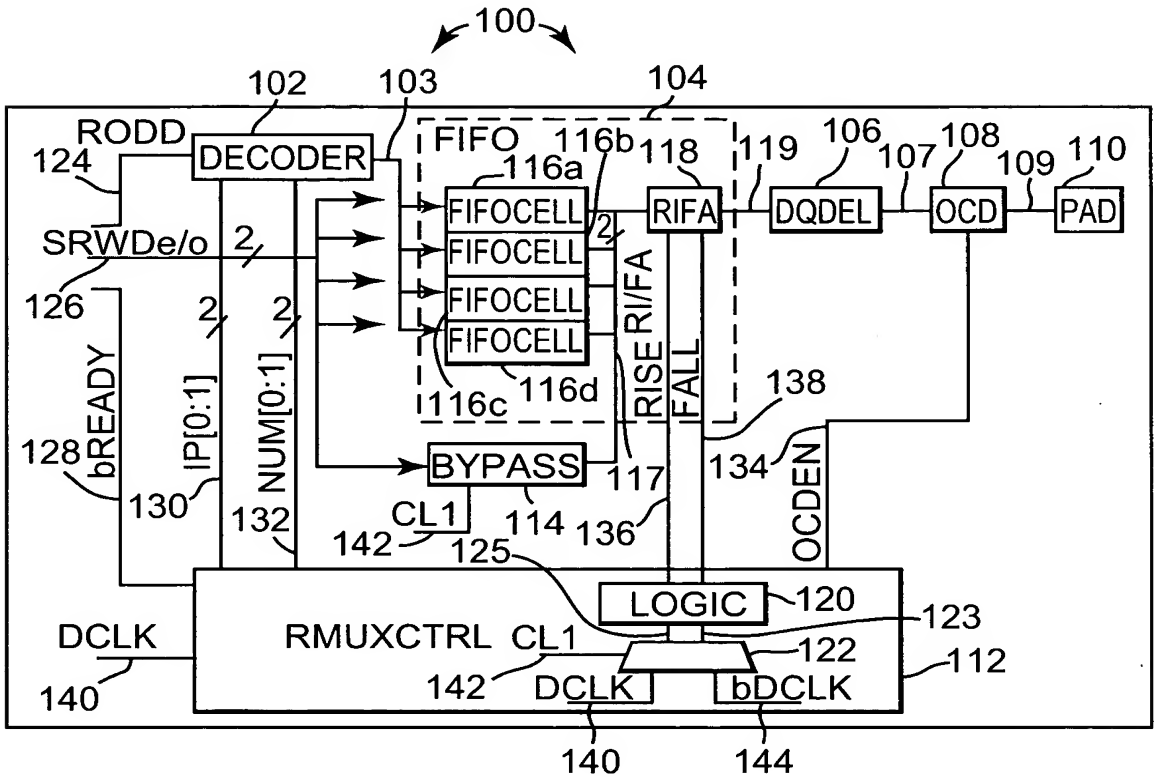
100
102
103
104
RODD
124
DECODER
FIFO
116b
116a
118
119
106
107
108
109
110
FIFOCELL
FIFOCELL
FIFOCELL
FIFOCELL
RIFA
DQDEL
OCD
PAD
SRWDe/o
2
126
2
2
RISE
RI/FA
IFALL
116c
116d
138
128
bREADY
IP[0:1]
NUM[0:1]
BYPASS
117
134
OCDEN
130
132
CL1
142
114
136
125
LOGIC
120
123
DCLK
RMUXCTRL
CL1
122
112
140
142
DCLK
bDCLK
140
144

Fig. 3

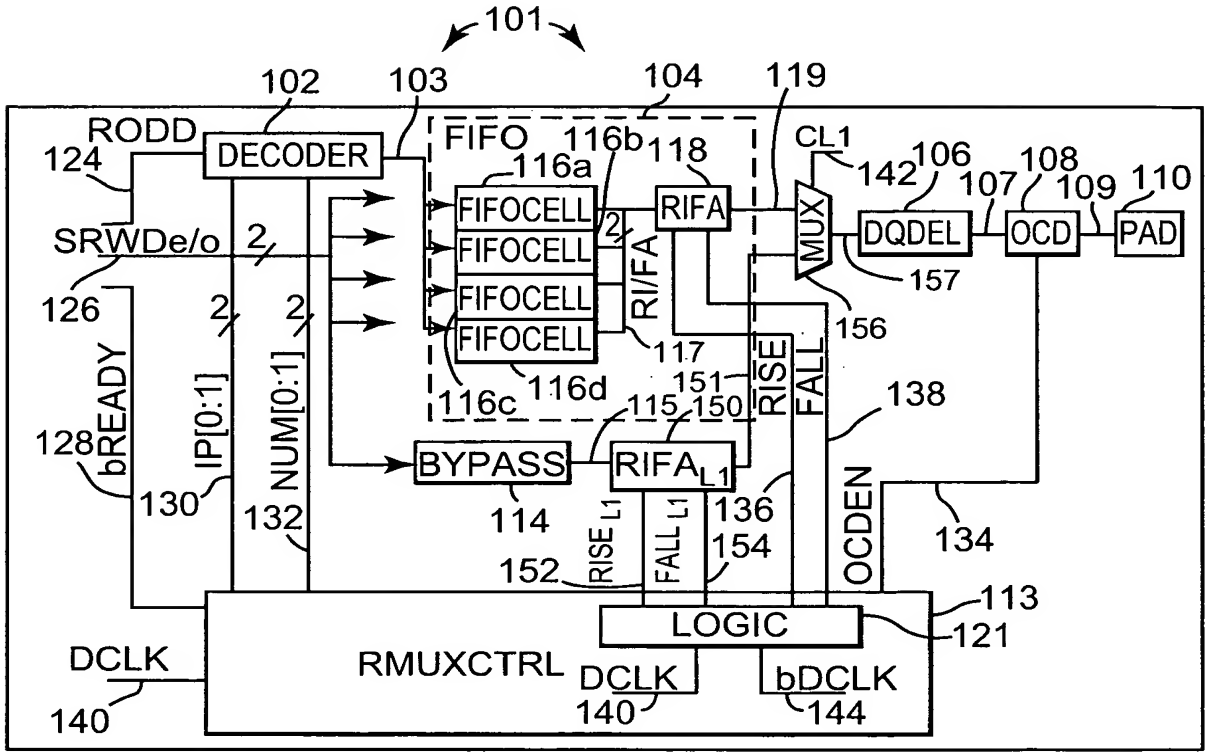
101
102
103
104
119
RODD
124
DECODER
FIFO
116b
118
CL1
142
106
108
107
109
110
116a
FIFOCELL
FIFOCELL
FIFOCELL
FIFOCELL
RIFA
MUX
DQDEL
OCD
PAD
SRWDe/o
2
RI/FA
126
2
2
157
156
117
116c
116d
151
115
150
RISE
FALL
138
128
bREADY
IP[0:1]
NUM[0:1]
BYPASS
RIFA L1
130
132
114
RISE L1
FALL L1
136
154
OCDEN
134
152
113
LOGIC
121
DCLK
RMUXCTRL
DCLK
bDCLK
140
140
144

Fig. 4

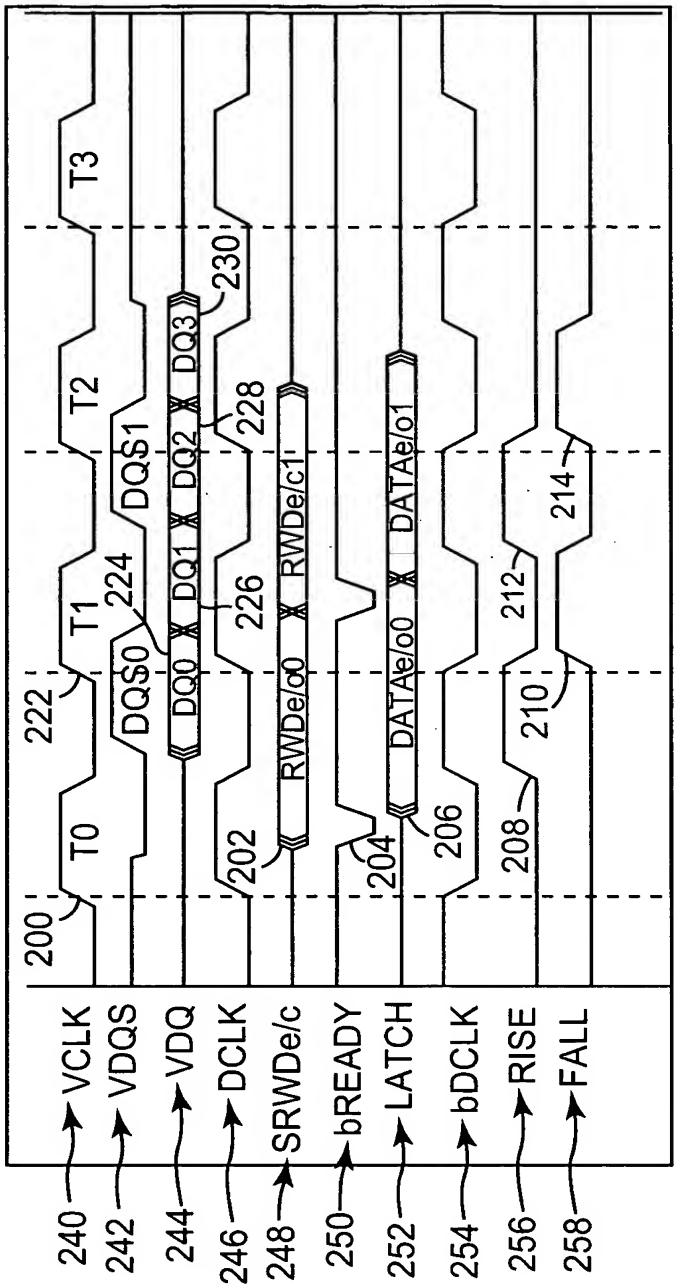
VCLK
VDQS
VDQ
DCLK
SRWDe/c
bREADY
LATCH
bDCLK
RISE
FALL
240
242
244
246
248
250
252
254
256
258
200
T0
T1
T2
T3
222
224
226
228
230
202
204
206
208
210
212
214
DQS0
DQS1
DQ0
DQ1
DQ2
DQ3
RWDe/o0
RWDe/c1
DATAe/o0
DATAe/o1

Fig. 5